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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,535	09/22/2003	Paul F. Illegems	5707-0410	9954

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Jeffrey C. Hood
Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,535	ILLEGEMS, PAUL F.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sep 22, 2003 & Jun 29, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06292004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because Fig. 7 should have the typo "ouput" in block 720 changed to --output--. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informality: Page 15, paragraph 0038, line 7 "gate and source" should be --gate and drain-- to accurately correspond to the connections of NMOS 504 shown in Fig. 6. An appropriate correction is required.

Claim Objections

Claims 2, 5, 7-8, 10, 13, 15, 18, 20, 22, and 24 are objected to because of the following informalities: Claim 2, line 5 "a constant" should be --the constant-- to clearly refer back to "a constant current sink" cited on line 2; lines 6 and 8 should have "current sink" preceded by --constant-- to provide consistent labeling throughout the claims, thus minimizing possible confusion; and line 10 should have --the-- added prior to "first" to refer back to "a first component" cited on line 6 of claim 1. Since claims 1, 9 and 16 each recite the variations in temperature and transistor fabrication parameters, it is suggested the term --the-- be added prior to "variations" on lines 2 and 3 of each of claims 5, 8, 13, 15, 18, 20, 22, and 24. Claim 7, line 2 "emitters" should be replaced with --sources-- because NMOS transistors do not have emitters. Claim 10 should be changed for the same reasons as applied to claim 2 above (i.e. line 5 "a constant" changed to --the constant--; lines 6 and 8 should --constant-- added prior to "current"; and line 10 should have --the-- added prior to "first." Related to the possibility that claims 2 and 10 could be incomplete (as described below with respect to each of the claims not ending with a period), it is suggested the last limitation recited within claims 2 and 10 be preceded by the term –and--. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Since each of claims 1, 2, 9, and 10 does not end with a period, it is not

understood if the claims are complete, or if any additional limitation was meant to be recited. For example, line 1 of each of claim 3, 4, 11, and 12 recites "the voltage generator further comprises", which implies independent claims 1 and 9 were meant to recite the voltage generator comprising/including some other element(s). However, although the voltage generator delivers a voltage in each of claims 1 and 9, it is not recited as comprising anything. Claim 2, line 7 is confusing because it is not clear if "the transistor" refers to one of the transistors recited within claim 1 (i.e. "NMOS tail current transistor" on line 2, or "NMOS transistors" on line 7), or to the "diode-connected NMOS transistor" on lines 1-2 and 4 of claim 2. It is not clear how the "differential pair of NMOS transistors" in claim 7 relates to the voltage level detector and NMOS transistors of claim 1 (e.g. see lines 2 and 7). Similar to claim 2 above, what does "the transistor" on line 7 of claim 10 refer to, the "tail current transistor" or "NMOS transistors" of claim 9, or the "diode-connected NMOS transistors" of claim 10?

Both claims 4 and 5 recite the limitations "the diode-connected NMOS transistor" and "the bandgap voltage reference" in lines 3-4 and 5, respectively. There is insufficient antecedent basis for these limitations in the claims' chain of dependency.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 8-9, 13, and 15-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu. In Fig. 1, Wu shows a device comprising a voltage level detector M7-M10 comprising NMOS tail current transistor M9; and voltage generator M1-M6 coupled to deliver a voltage (on line 12) to the gate of tail current transistor M9. The voltage comprises a first component (e.g. threshold voltage of diode-connected NMOS transistor M3) approximately equal to the threshold voltage of NMOS transistors (e.g. M3-M10) within the device; and a second component (e.g. threshold voltage of diode-connected NMOS transistor M4) of the voltage is considered approximately constant with respect to variations in operating temperature as well as transistor fabrication parameters. Therefore, claim 1 is anticipated. Since the first component (e.g. threshold voltage of M3) of the voltage makes the voltage on line 12 substantially equivalent to 2 x Vtn, this will turn tail current transistor M9 on despite variations in operating temperature and transistor fabrication parameters, anticipating claim 5. By re-identifying voltage level detector M7-M10 as a differential amplifier comprising NMOS tail current transistor M9, claims 9, and 13 are anticipated for the same reasons as claims 1 and 5 described above. In yet another interpretation of the Fig. 1 circuit, one of ordinary skill in the art would understand the circuit corresponds to a method for generating a constant reference voltage (i.e. diode-configured M4 provides a voltage equivalent to one NMOS threshold); generating a voltage that approximates the threshold voltage of an NMOS process (i.e. diode-configured M3 provides another voltage equivalent to an NMOS threshold); and the sum of the constant reference voltage and approximate threshold voltage generate a composite voltage on line 12. Since M3 is a diode-configured NMOS transistor, it will inherently provide its threshold voltage of an NMOS process over variation in operating temperature as well as variation in transistor fabrication parameters.

[Note: Wu also discloses the bias current is fairly independent of variations in voltage, process parameters, and temperature. See column 5, lines 45-49.] Therefore, claim 16 is anticipated. The composite voltage (e.g. 2 x Vtn) on line 12 is applied to the gate of tail current transistor M9 of voltage level detector M7,M8, which one of ordinary skill in the art would also understand is a differential amplifier. Thus, claims 17 and 21 are also anticipated. Since the threshold component (from M3) of the composite voltage makes the voltage on line 12 equivalent to 2 x Vtn, this will turn tail current transistor M9 on despite variations in operating temperature and transistor fabrication parameters, anticipating claim 18. With M4 being an NMOS transistor configured as an input transistor of current mirror M4,M10 that has output current mirror transistor M10 coupled in series with tail current transistor M9, the constant reference component (from M4) will produce a tail current for voltage level detector M7,M8 that is proportional to beta for the NMOS process, and claim 19 is anticipated. By maintaining a constant tail current, the trip point/offset voltage of the voltage level detector/differential amplifier will be approximately constant despite variations in operating temperature and transistor fabrication parameters, anticipating claims 8, 15, and 20. Claims 22-24 are anticipated for the same reasons as previously described (e.g. see claims 5, 13, 15, and 19-20).

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 2-4, 6-7, 10-12, and 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. [Note: Some of the rejections may have been carried over from claim(s) upon which they depend.] There is presently no

strong motivation to combine or modify any prior art reference(s) to ensure the device comprises: 1) the first component of the voltage is produced by a diode-connected NMOS transistor and a constant current sink as recited within claims 2 and 10; 2) a bandgap voltage reference produces the second component of the voltage as recited within claims 3 and 11; 3) an amplifier and PMOS transistor produce the sum of the first/second components as recited within claims 4 and 12; 4) the second component is a constant effective voltage, wherein the tail current is proportional to beta according to the equation recited within claims 6 and 14; and 5) the channel width to length ratios of the first and second transistors differ as recited within claim 7.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed inventions. Although not used in any formal rejection described above, the following references should be carefully reviewed and considered. Kanda et al. shows a circuit in Fig. 3 that one of ordinary skill in the art would recognize as having Vref and Qn4 generating a constant reference voltage (e.g. between Qn3 and Qn4); diode-connected Qn3 generates a threshold voltage of an NMOS process; and Vref' is a composite voltage of the constant reference voltage and the threshold voltage. Fig. 4 of Kanda et al. shows composite voltage Vref' being generated with respect to diode-connected transistors Qn3,Qn4, current source Qn5, amplifier AMP, reference voltage Vref, and PMOS transistor Qp3. Transistor Qn6 could be used as a tail current transistor to provide current Iref to a voltage detector/differential amplifier. Fig. 9 of Chevallier shows a current reference circuit that could be used to provide tail current to a voltage level detector/differential amplifier. The circuit comprises a constant reference voltage VREF (inherently provided by some type of voltage generator); diode-

connected NMOS transistor 31 that provides an NMOS threshold voltage; and the voltage between R3 and 31 is a composite voltage comprising the constant reference voltage and the threshold voltage. This voltage is applied to the gate of transistor 28, which could be used as the tail current transistor.

The prior art references cited on the IDS submitted Jun 29, 2004 were reviewed and considered. None of these references clearly shows or discloses a (composite) voltage as recited within the independent claims, wherein the voltage comprises an approximate threshold voltage of an NMOS transistor, plus a constant (reference) voltage.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
15 December 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800